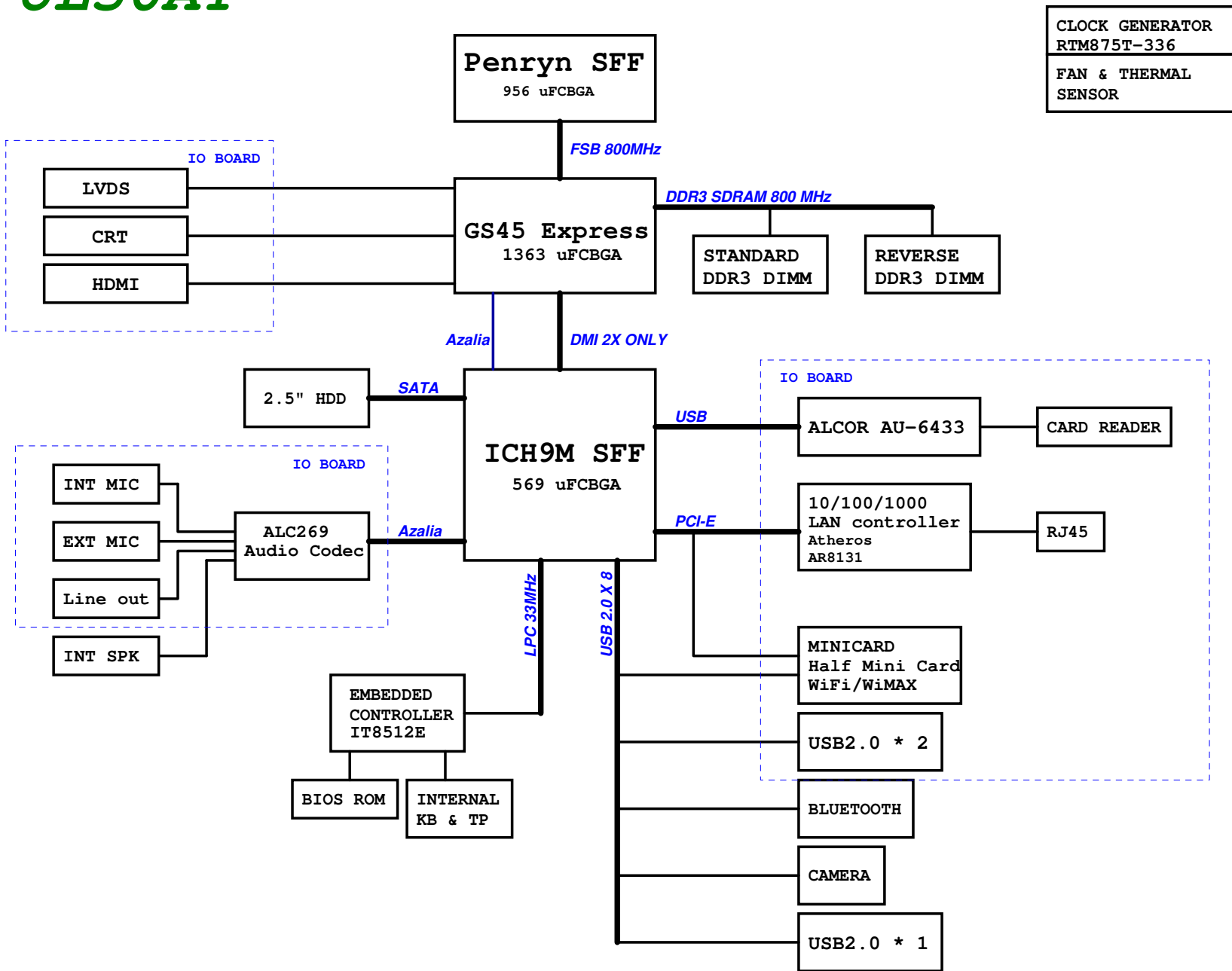


UL50AT

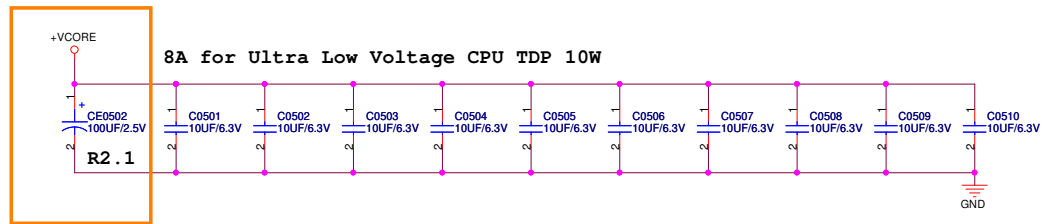


POWER

VCORE
SYSTEM
I/O_1.05VS
I/O_DDR & VTT
I/O_+1.8VS
CHARGER

[illegible][illegible]

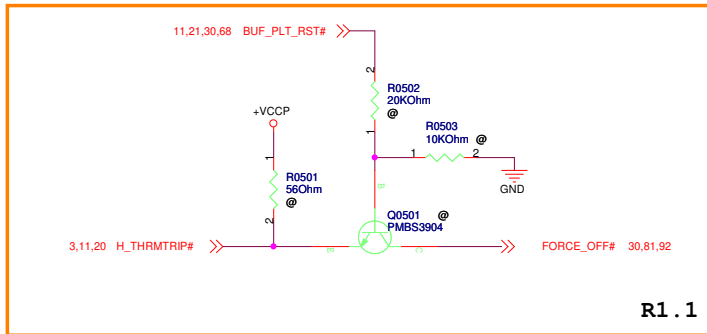
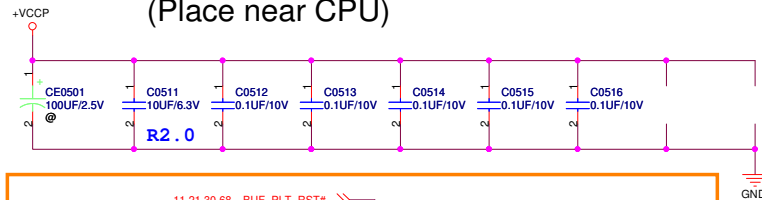




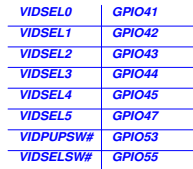
Decoupling guide from Intel

VCCORE	10uF	mount	*4pcs
	0.1uF	mount	*5pcs
VCCP	1uF		*12pcs
	270uF		*1pcs
VCCA	0.01uF		*1 pcs
	10uF		*1 pcs

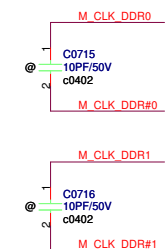
+VCCP Decoupling Capacitor (Place near CPU)



<Variant Name>



Place near SO-DIMM_0



13 M_A_DQS[7:0] << >> M_A_DQS[7:0]
13 M_A_DQS# [7:0] << >> M_A_DQS# [7:0]

13 M_A_DM[7:0] << >>

8,22,24,29 SMB_CLK_S << >>
8,22,24,29 SMB_DAT_S << >>

11 M_CLK_DDR1
11 M_CLK_DDR#1
11 M_CLK_DDR0
11 M_CLK_DDR#0
11 M_CS#1
11 M_CS#0
11 M_ODT1
11 M_ODT0
13 M_A_WE#
13 M_A_RAS#
13 M_A_CAS#
13 M_A_BS2
13 M_A_BS1
13 M_A_BS0
11 M_CKE1
11 M_CKE0

GND

SA1

SA0

M_A_DQS7

M_A_DQS#7

M_A_DQS6

M_A_DQS#6

M_A_DQS5

M_A_DQS#5

M_A_DQS4

M_A_DQS#4

M_A_DQS3

M_A_DQS#3

M_A_DQS2

M_A_DQS#2

M_A_DQS1

M_A_DQS#1

M_A_DQS0

M_A_DQS#0

M_A_DM7

M_A_DM6

M_A_DM5

M_A_DM4

M_A_DM3

M_A_DM2

M_A_DM1

M_A_DM0

13 M_A_DQ[0..63] << >> M_A_DQ[0..63]

U0701A
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10/AP
A11
A12/BC#
A13
A14
A15

CK1

CK1#

CK0

CK0#

S1#

S0#

ODT1

ODT0

WE#

RAS#

CAS#

BA2

BA1

BA0

CKE1

CKE0

SA1

SA0

M_A_DQS7

M_A_DQS#7

M_A_DQS6

M_A_DQS#6

M_A_DQS5

M_A_DQS#5

M_A_DQS4

M_A_DQS#4

M_A_DQS3

M_A_DQS#3

M_A_DQS2

M_A_DQS#2

M_A_DQS1

M_A_DQS#1

M_A_DQS0

M_A_DQS#0

M_A_DM7

M_A_DM6

M_A_DM5

M_A_DM4

M_A_DM3

M_A_DM2

M_A_DM1

M_A_DM0

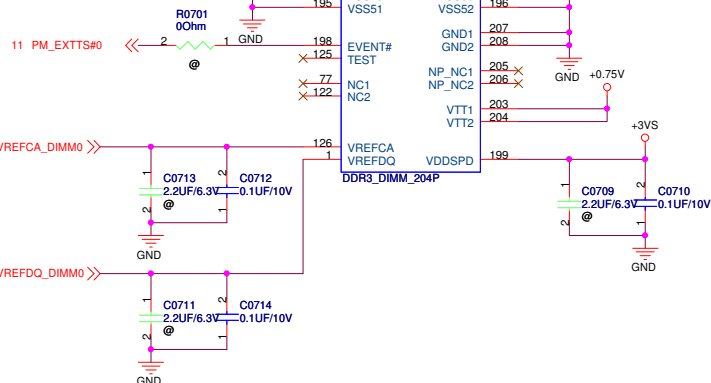
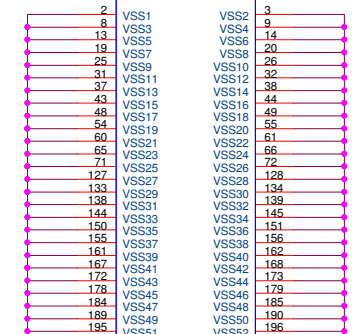
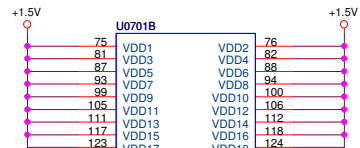
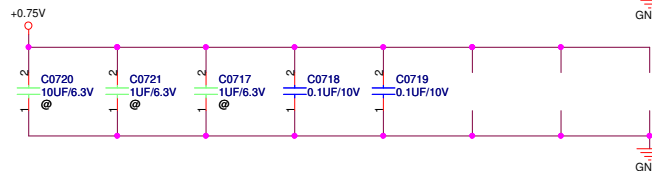
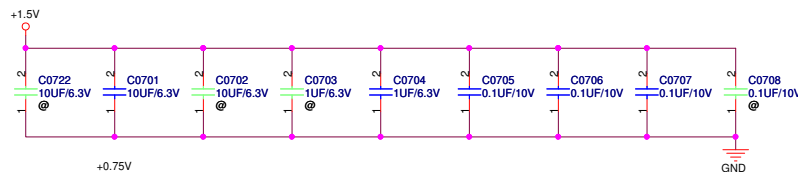
RESET#

SDA

DDR3_DIMM_204P

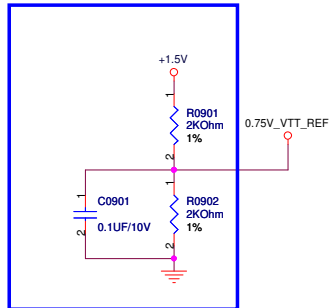
12G02553204W

DDR3 DIMM 204P,1.5V,5.2H,REV

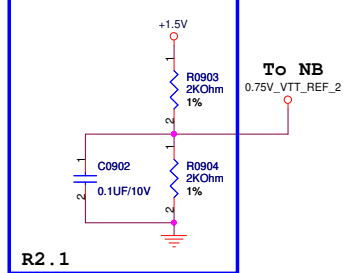


<Variant Name>

R2.1

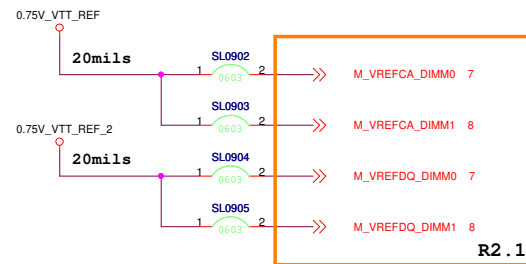
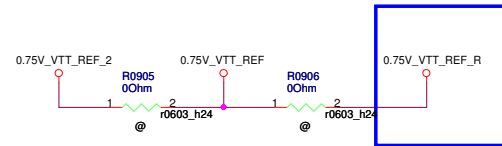


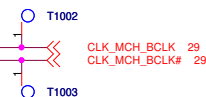
Place Close to NB

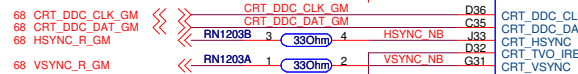
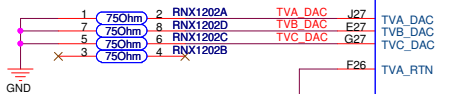
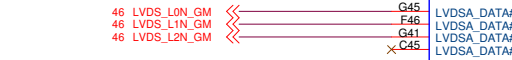
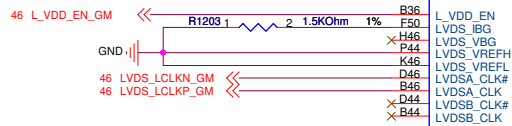
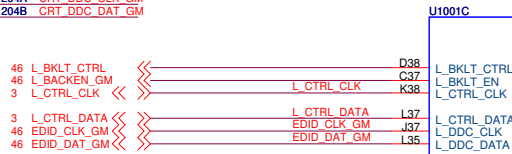
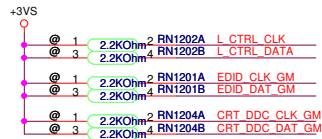


R2.1

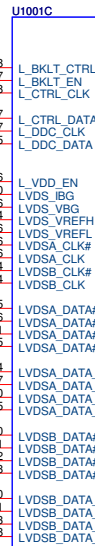
From DDR/VTT Power Circuit



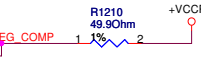
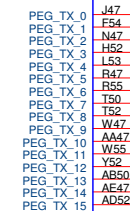
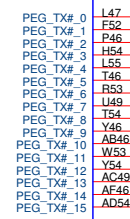
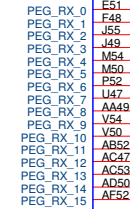
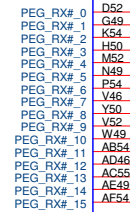




Check : R1208
如果CRT Trace 12"以内,放1kohm
如果CRT Trace 12~15.3",放976ohm



GRAPHICS
PCI-EXPRESS
VGA



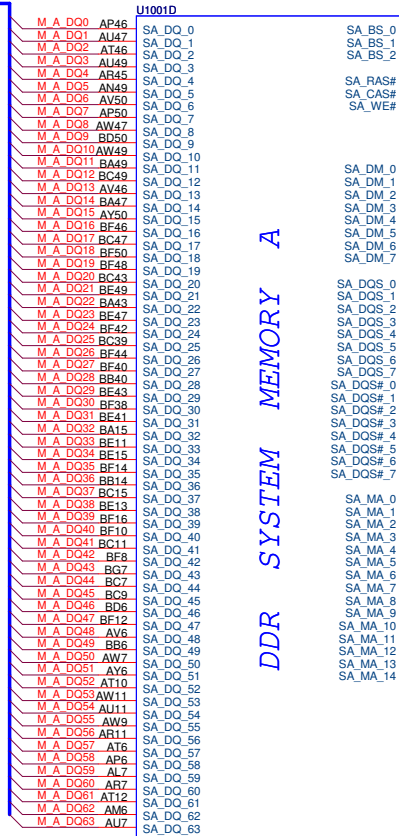
<Variant Name>

ASUS Title : NB GS45 DISPLAY
ASUSTeK COMPUTER INC. Engineer: Jack Hsu

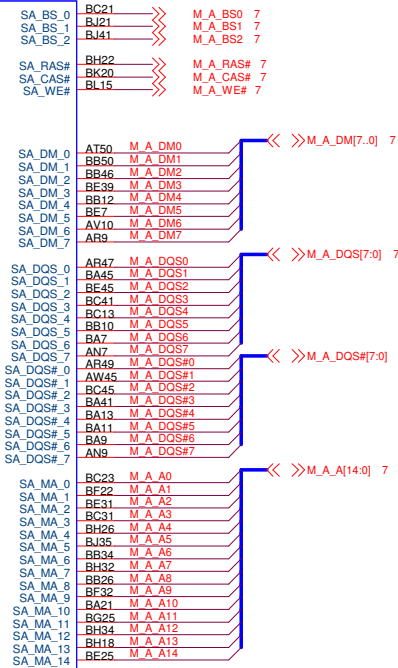
Size Project Name
Custom UL50AT Rev 2.0

Date: Friday, October 16, 2009 Sheet 12 of 97

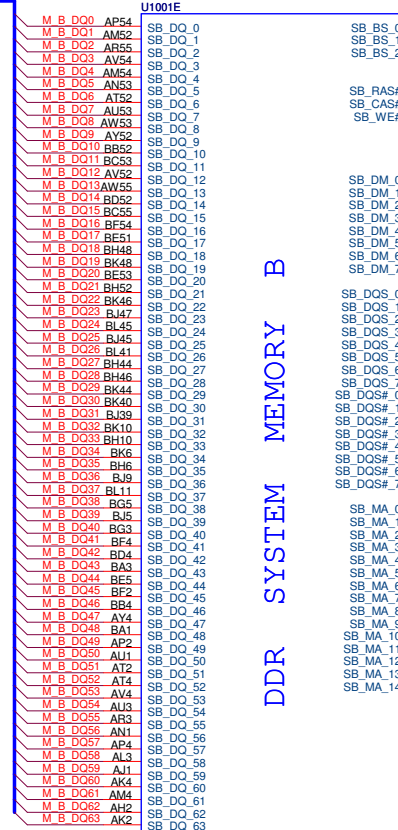
7 M_A_DQ[63:0] << >>



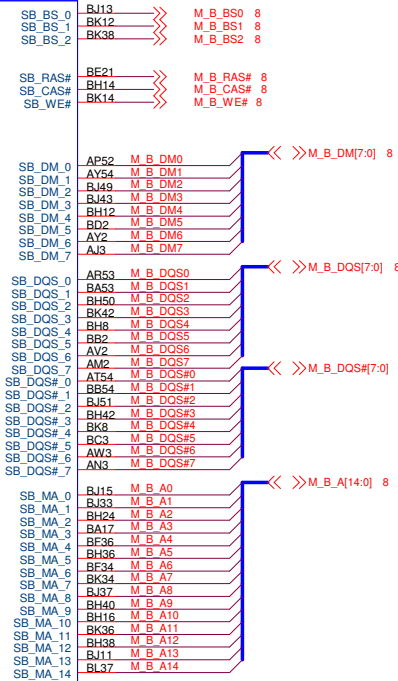
DDR SYSTEM MEMORY A



8 M_B_DQ[63:0] << >>



DDR SYSTEM MEMORY B



<Variant Name>

+1.5V_GMCH

+VGFX_CORE

+VGFX_CORE

3060mA
+VCC_GMCH

R1.1

POSICAP 100UF/4V (3528/B2) 20%
R1.1

R1.1

POSICAP 100UF/4V (3528/B2) 20%
R1.1

R2.1

POSICAP 100UF/4V (3528/B2) 20%
R1.1

For SFF
5739mA
+VGFX_CORE

+1.5V_GMCH

+VCC_GMCH

VCC CORE

POWER

VCC NCTF

POWER

VCC SM

VCC GFX NCTF

VCC GFX

VCC GFX

VCC SM IF

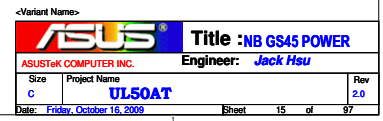
R1.1

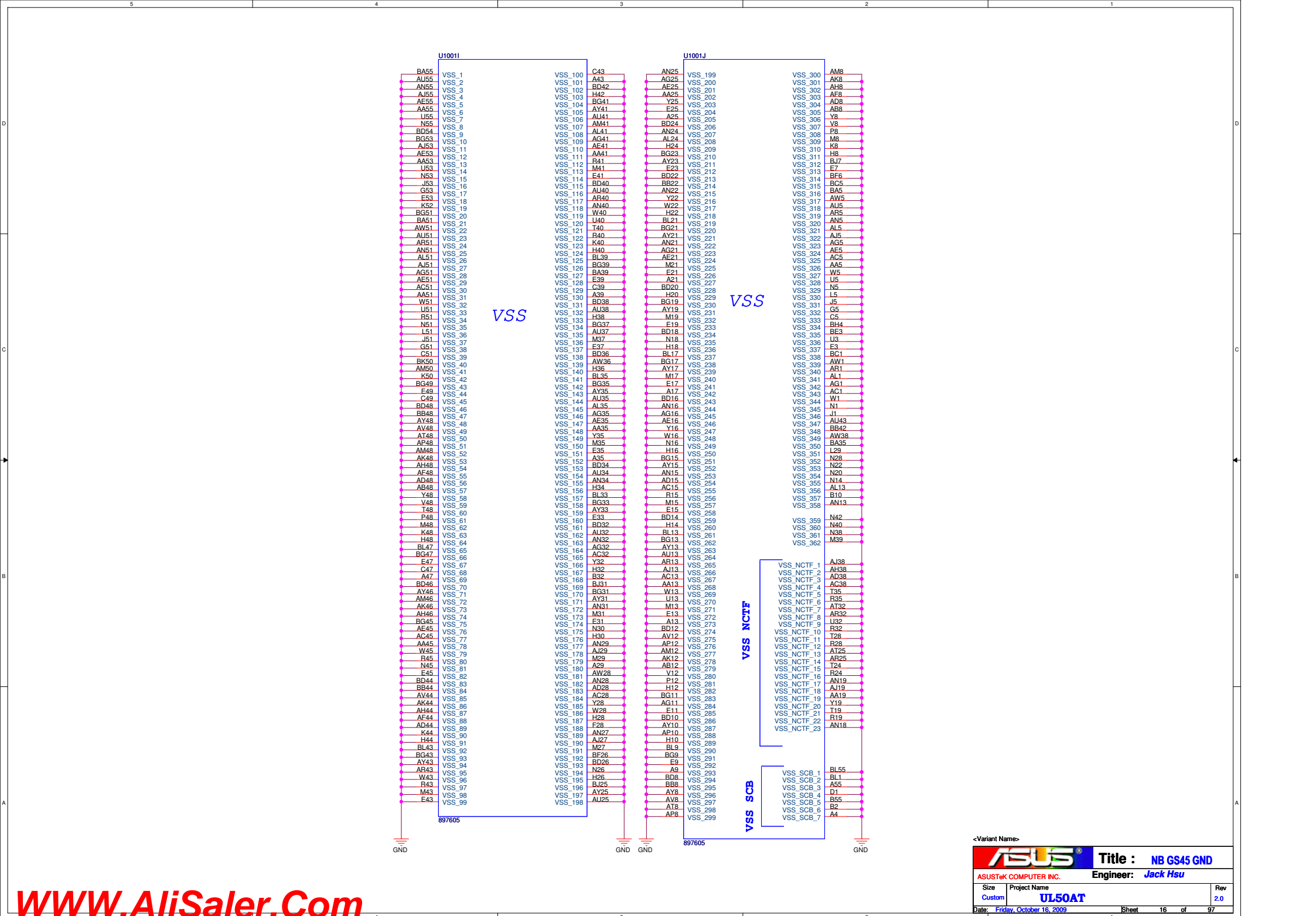
Route VCC_AKG_SENSE and
VSS_AKG_SENSE differentially.

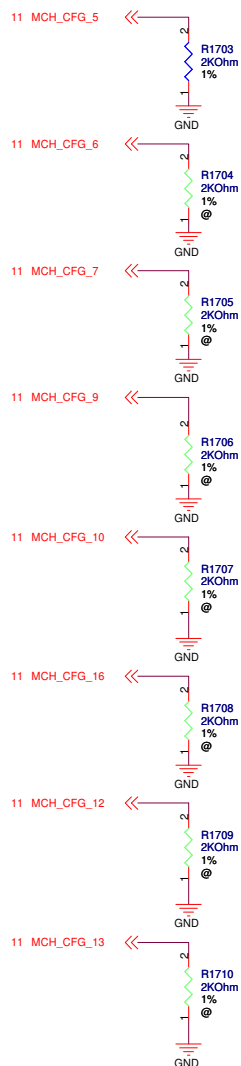
897605

897605

ASUS Logo
Title : NB GS45 POWER
ASUSTek COMPUTER INC. Engineer: Jack Hsu
Size C Project Name UL50AT Rev 2.0
Date: Friday, October 16, 2009 Sheet 14 of 97







CFG5 : DMI STRAP

H = DMI X 4 (Default)
L = DMI X 2

CFG6 : ITPM Host Interface (Relate to SPI_MOSI)

H = ITPM Disable (Default)
L = ITPM enable (Can disable by SW)

CFG7 : Intel ME Crypto Strap

H = With confidentiality (Default)
L = Without confidentiality

CFG9 : PCIE Graphic Lane Reverse

H = Normal (Default)
L = Lanes Reverse

CFG10 : PCIE Loopback

H = Disable (Default)
L = Enable

CFG16 : FSB Dynamic ODT

H = Enable (Default)
L = Disable

CFG12 : ALL-Z Mode

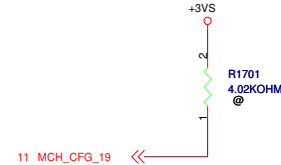
H = Disable (Default)
L = Enable

CFG13 : XOR Mode

H = Disable (Default)
L = Enable

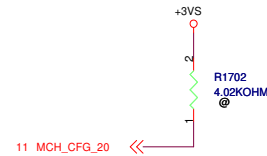
CFG [13:12] : XOR/ALL-Z

00 = Reserved
01 = XOR Mode Enabled
10 = All-Z Mode Enabled
11 = Normal Operation (Default)



CFG19 : DMI Lane Reversal

H = DMI Lane Reversal
L = Normal (Default)



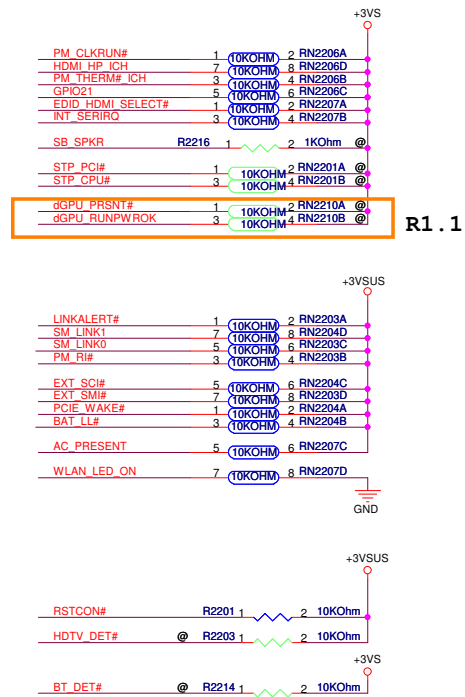
CFG20 : SDVO/PCIE CONCURRENT MODE

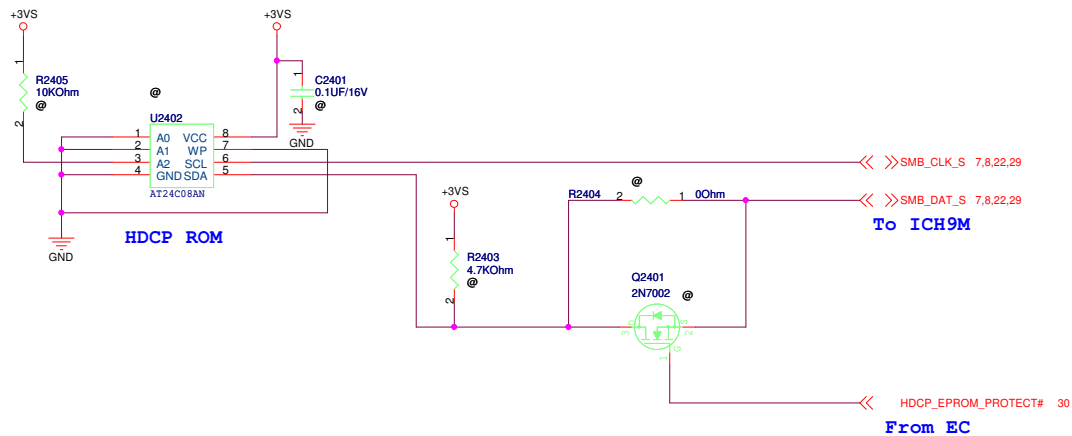
L = Only Digital display port or PCIE is Operational (Default)

H = Digital display port and PCIE are operating simultaneously via the PEG port

<Variant Name>







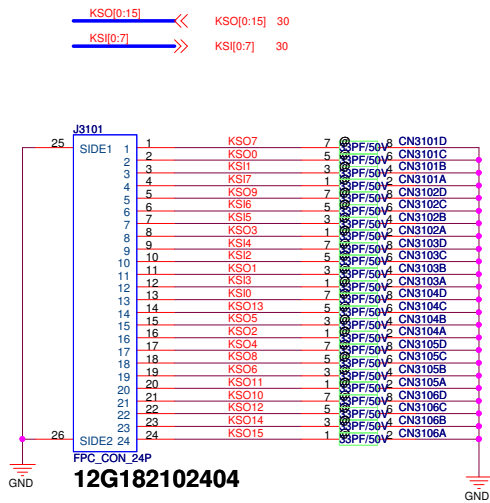
<Variant Name>

ASUS		Title : SB ICH9M (5)	
ASUSTeK COMPUTER INC.		Engineer: Jack Hsu	
Size	Project Name		Rev
Custom	UL50AT		2.0
Date: Friday, October 16, 2009		Sheet	24 of 97

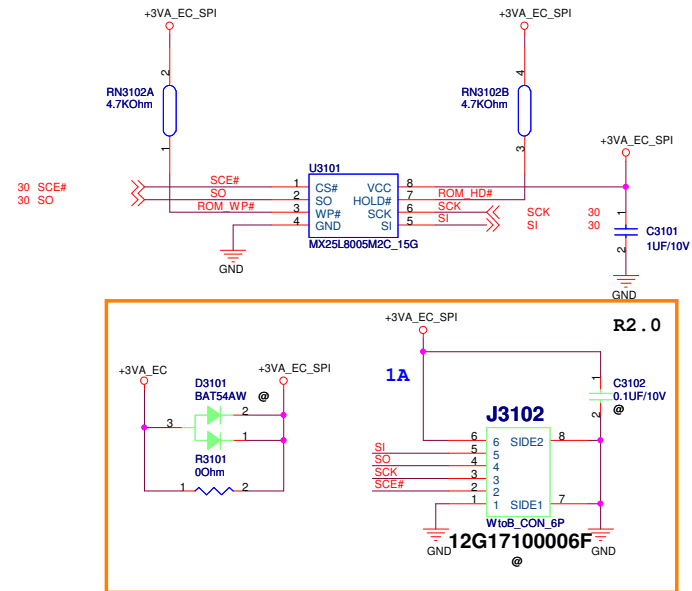





Internal Keyboard



SPI Flash ROM (8Mb)

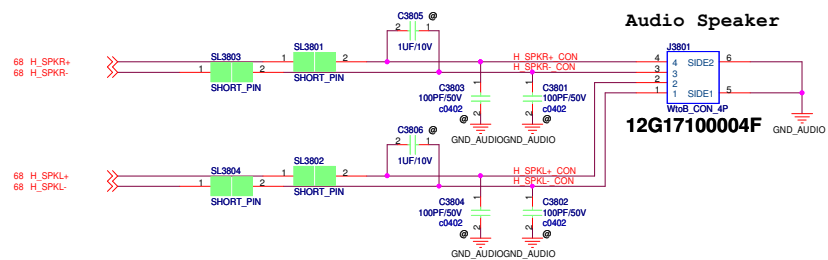


<Variant Name>

ASUSTeK COMPUTER INC.

Engineer: Jack Hsu

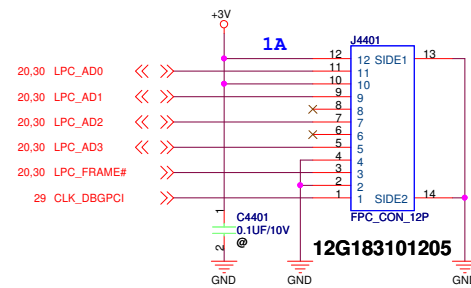
Size	Project Name	Rev
C	UL50AT	2.0
Date: Friday, October 16, 2009		Sheet 32 of 97








LPC DEBUG PORT



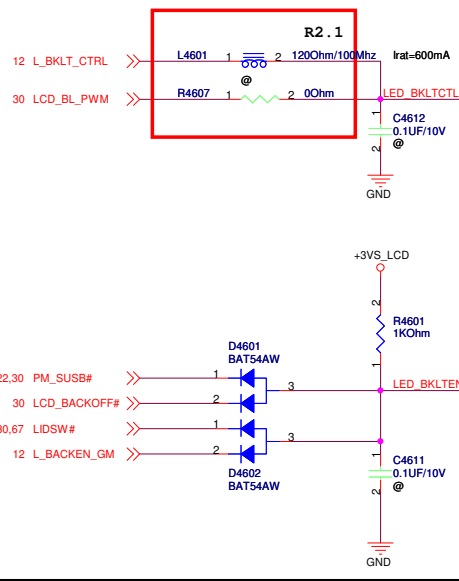
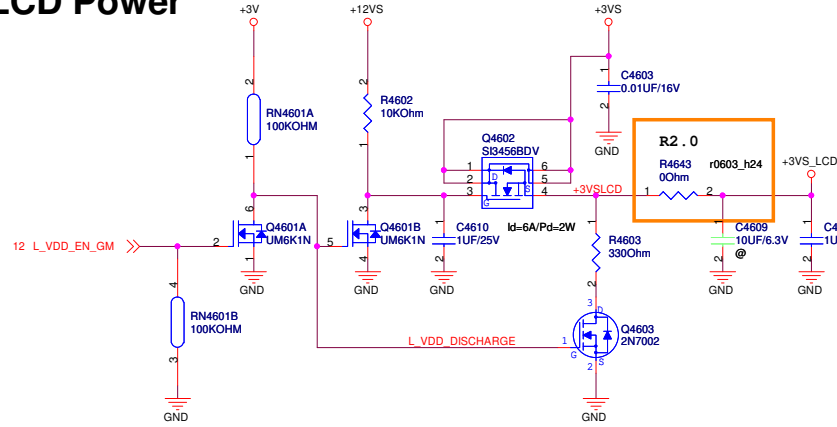
<Variant Name>

ASUS		Title : DEBUG PORT	
ASUSTeK COMPUTER INC.		Engineer: Jack Hsu	
Size	Project Name		Rev
Custom	UL50AT		2.0
Date: Friday, October 16, 2009	Sheet	44 of	97

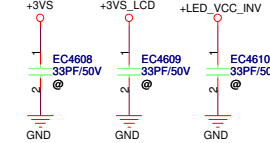
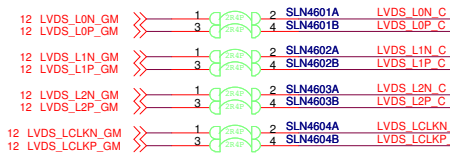
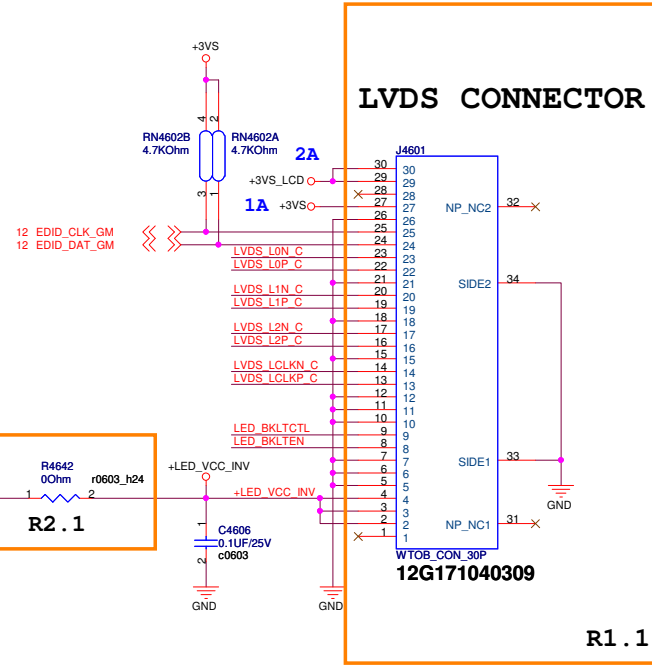
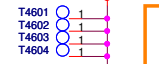
	5	4	3	2	1
D					
C					
B					
A					
	5	4	3	2	1

<Variant Name>		Title :<Title>	
		Engineer: Jack Hsu	
Size	Project Name		Rev
C	UL50AT		2.0
Date: Friday, October 16, 2009		Sheet	45 of 97

LCD Power

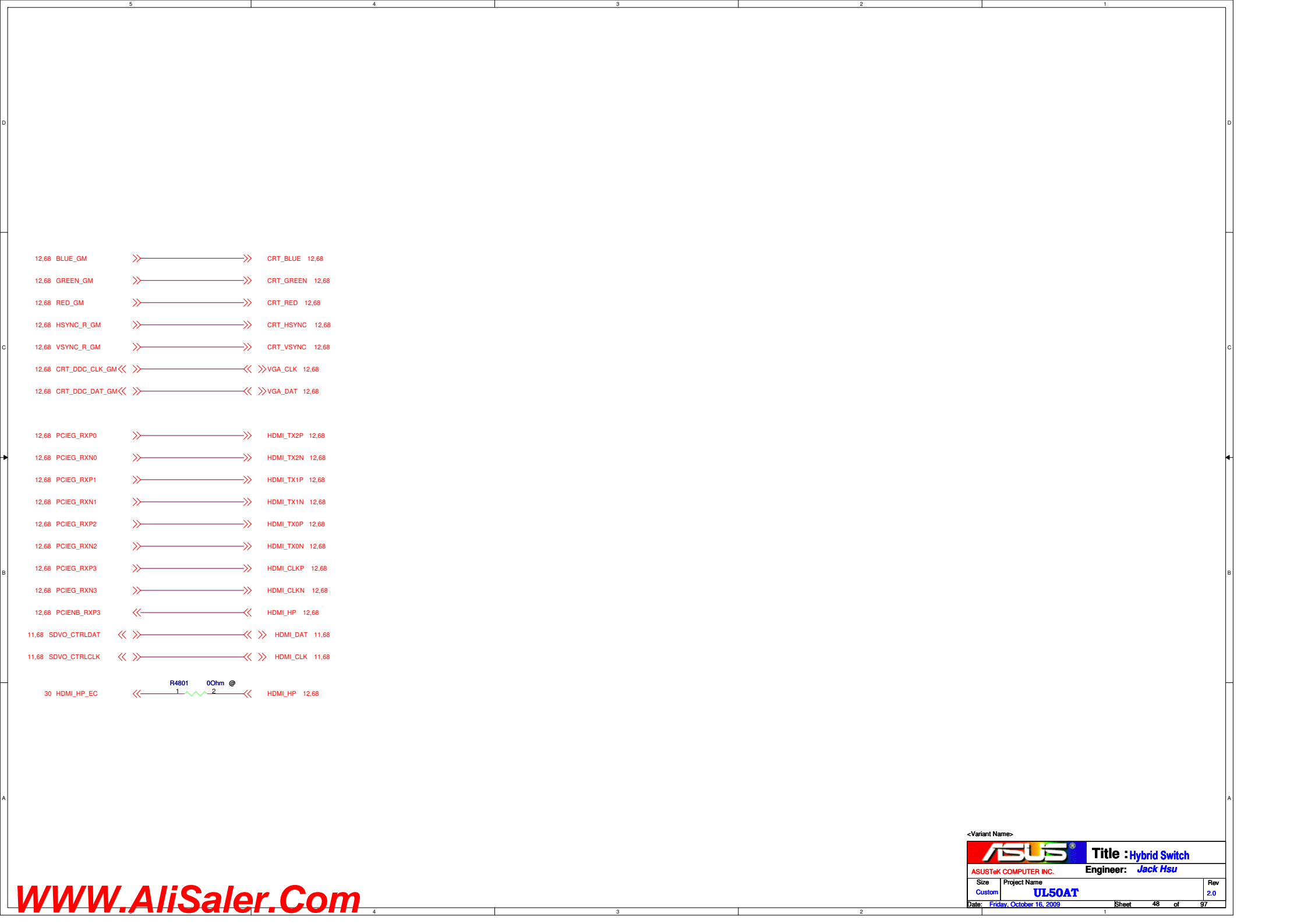


AC_BAT_SYS



	5	4	3	2	1
D					
C					
B					
A					
	5	4	3	2	1

<Variant Name>		Title :<Title>	
ASUSTeK COMPUTER INC.		Engineer: Jack Hsu	
Size	Project Name	Rev	
C	UL50AT	2.0	
Date: Friday, October 16, 2009		Sheet	47 of 97



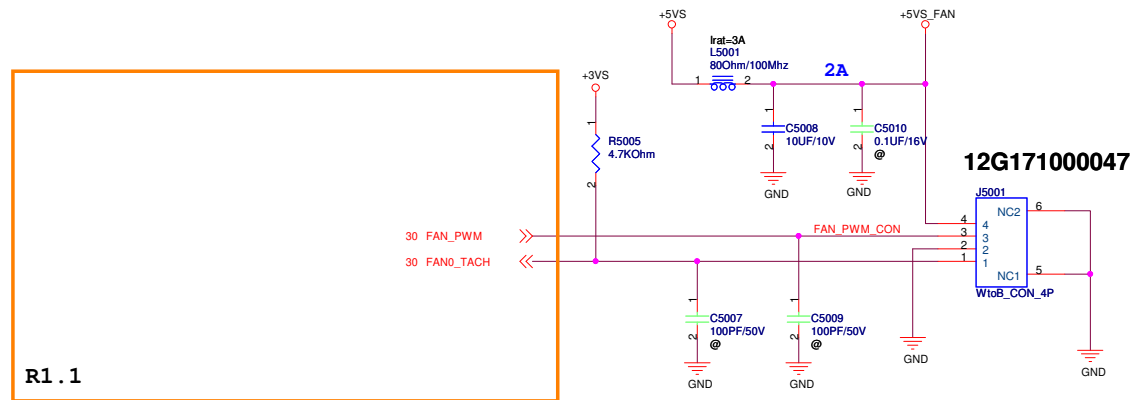
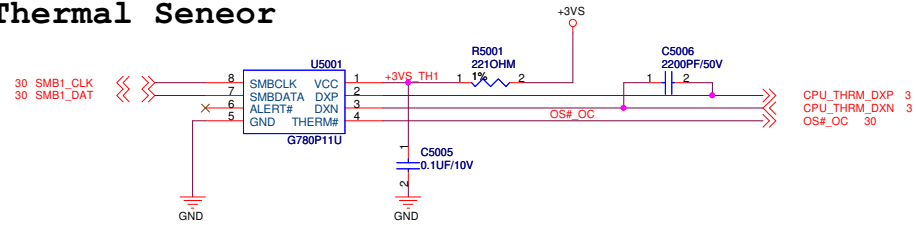
1nd: 06G023096010 G780P11U SOP-8
 2nd: 06G023026012 MAX6657YMS+ SOP-8

Route CPU_THRM_DA , CPU_THRM_DC and
 MEM_THERM_DA , MEM_THERM_DC on
 the same layer

-----OTHER SIGNALS
 10 mils
 =====GND
 10 mils
 =====H_THERMDA(10 mils)
 10 mils
 =====H_THERMDC(10 mils)
 10 mils
 =====GND
 10 mils
 -----OTHER SIGNALS

Avoid FSB,Power

Thermal Seneor

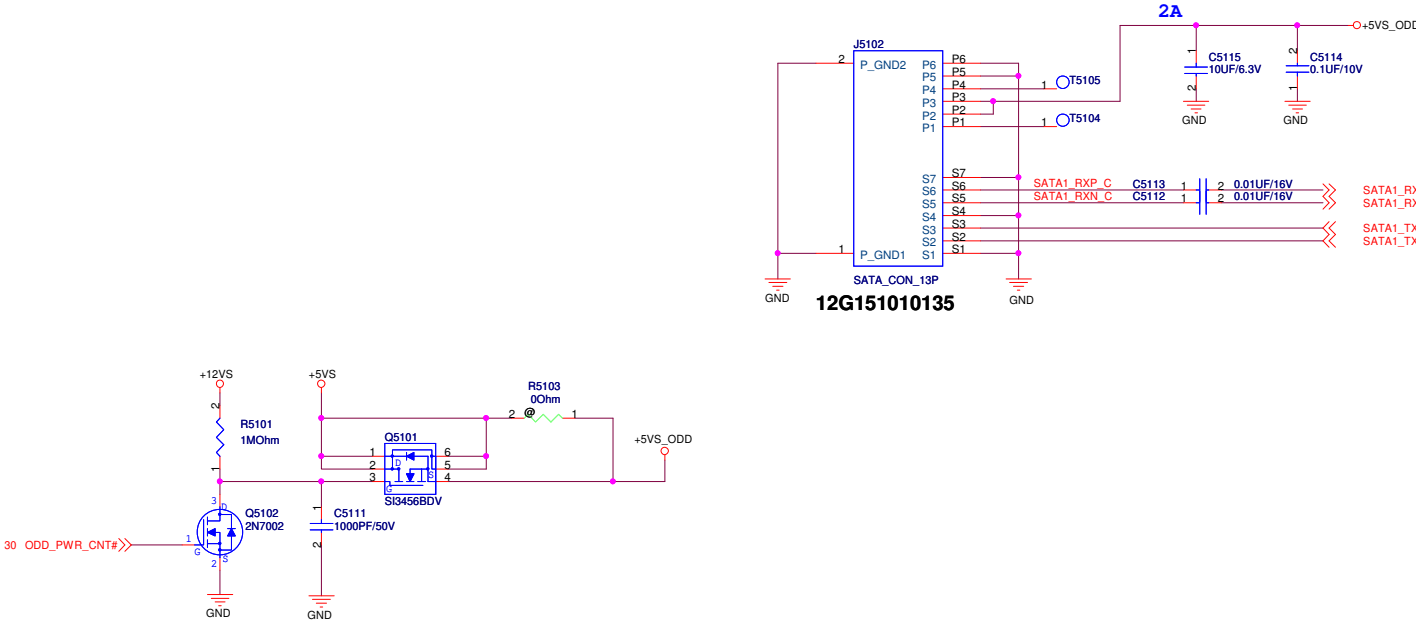
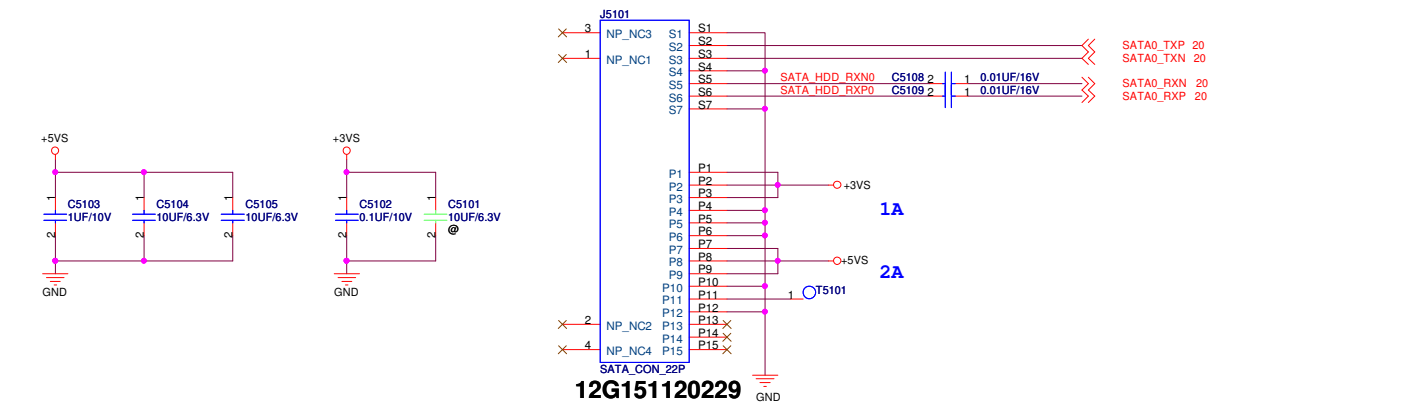


<Variant Name>

ASUS		Title : THERMAL & FAN	
ASUSTeK COMPUTER INC.		Engineer: Jack Hsu	
Size	Project Name		Rev
Custom	UL50AT		2.0
Date: Friday, October 16, 2009		Sheet	50 of 97

SATA HDD

SATA ODD







5

4

3

2

1

D

D

C

C

B

B

A

A

4

3

2

1

<Variant Name>



Title : LID

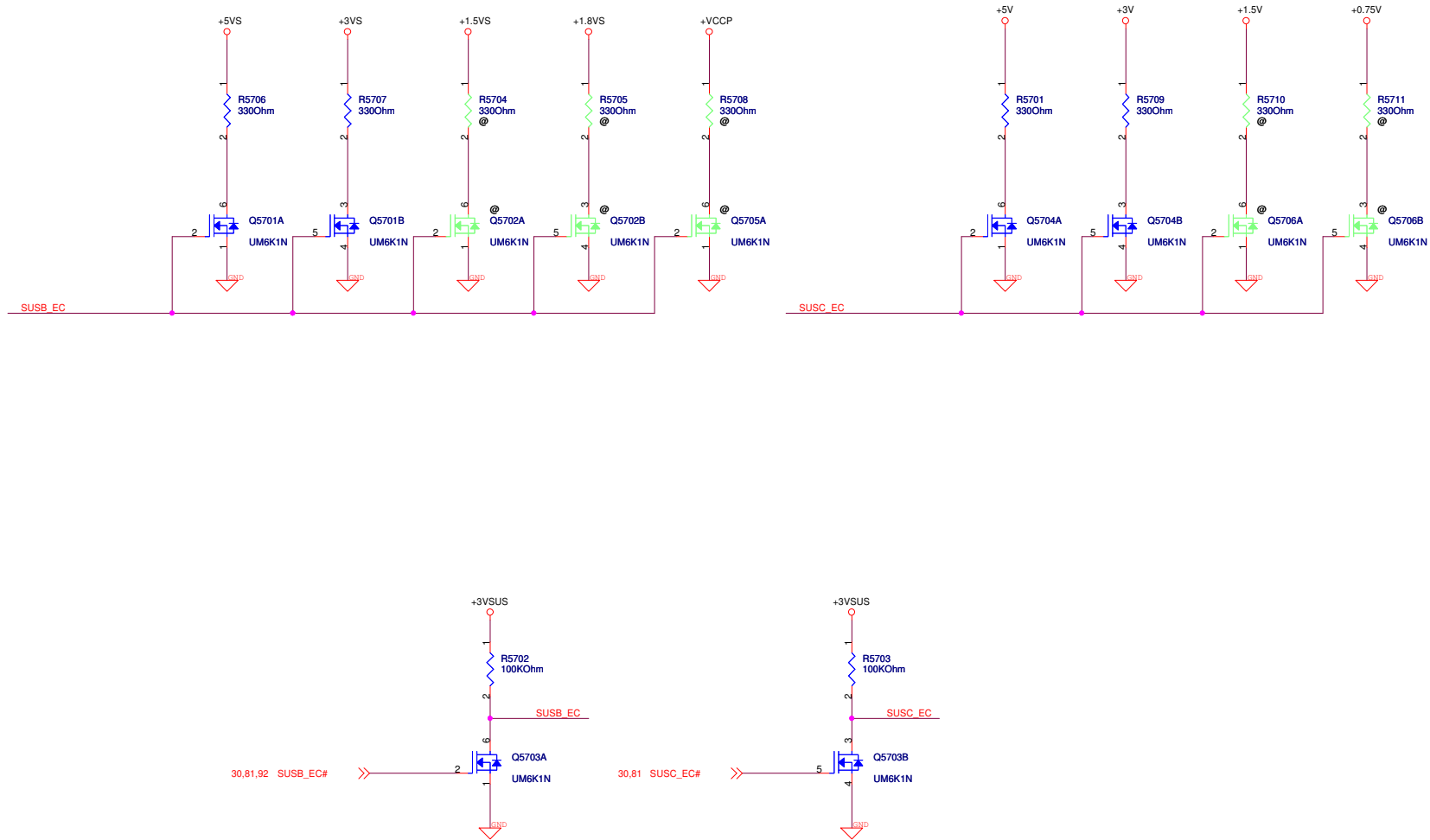
ASUSTeK COMPUTER INC.

Engineer: Jack Hsu

Size	Project Name	Rev
Custom	UL50AT	2.0

Date: Friday, October 16, 2009Sheet 56 of 97

Discharge Circuit

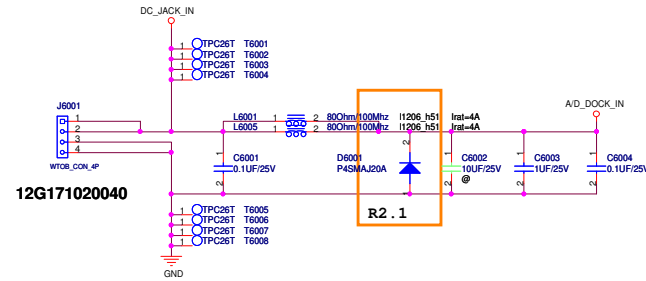


<Variant Name>

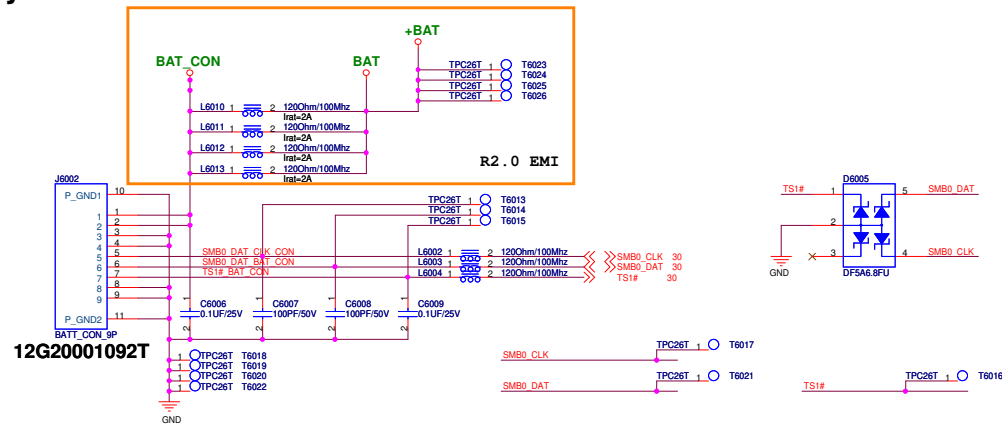
ASUS		Title DISCHARGE CIRCUIT	
ASUSTeK COMPUTER INC.		Engineer: Jack Hsu	
Size	Project Name		Rev
Custom	UL50AT		2.0
Date: Friday, October 16, 2009		Sheet	57 of 97



DC-IN



Battery Connector

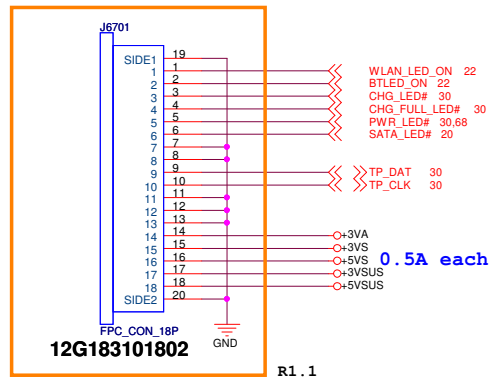




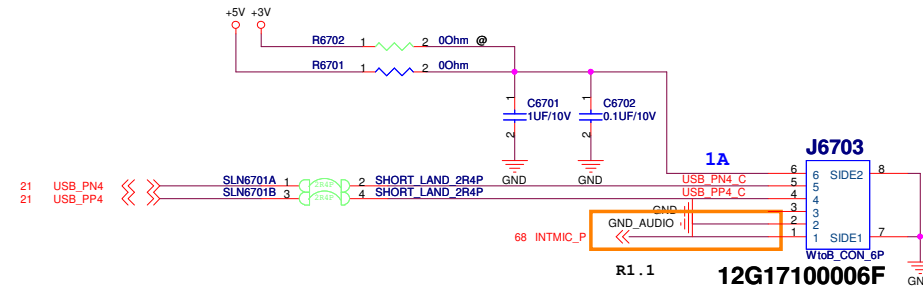
max. 60mA



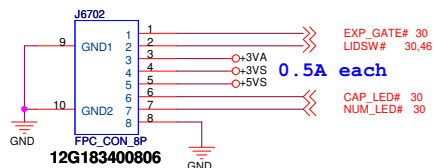
Touch Pad / LED Board



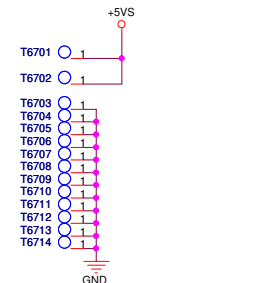
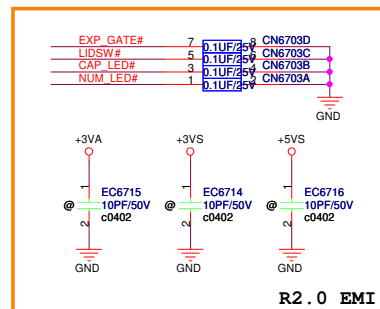
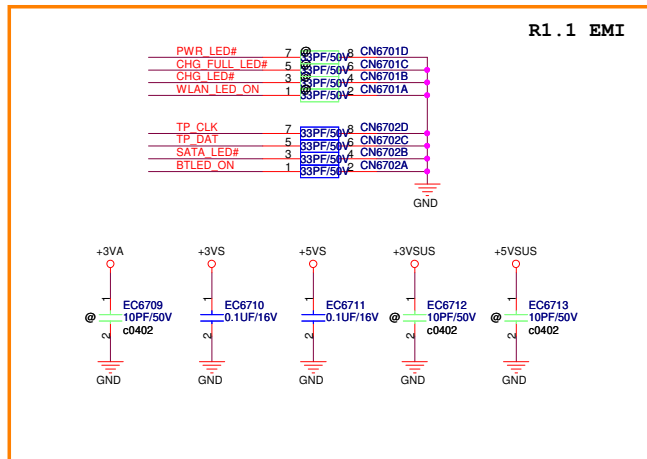
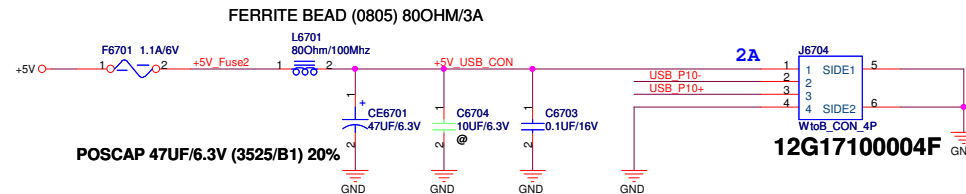
Camera Module



Function Board



FLY USB Cable

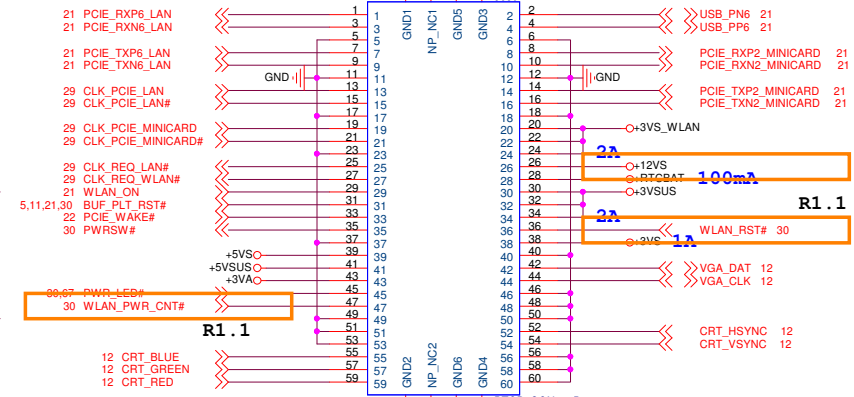
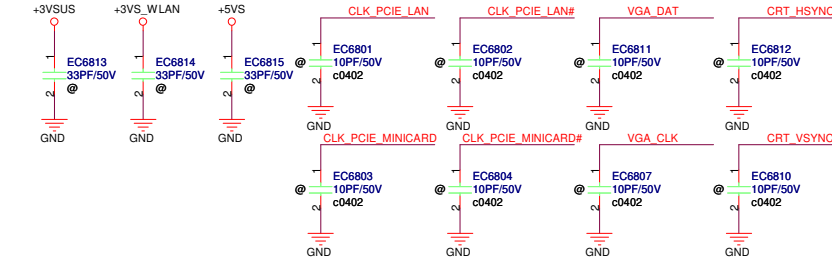
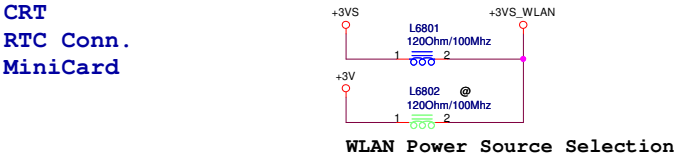


<Variant Name>

ASUS		Title : SUB BOARD	
ASUSTeK COMPUTER INC.		Engineer: Jack Hsu	
Size	Project Name	UL50AT	Rev 2.0
Custom			
Date: Friday, October 16, 2009		Sheet 67	of 97

IO BOARD - 02

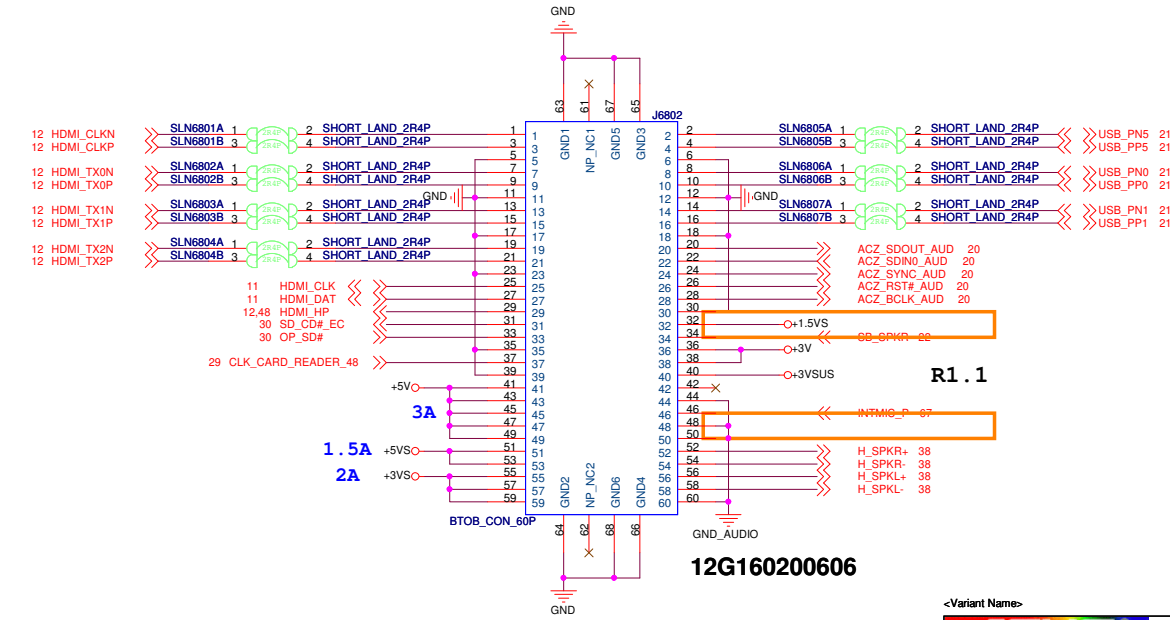
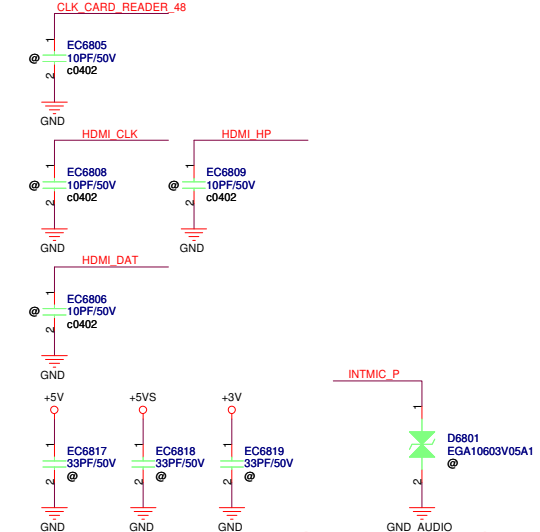
LAN IC
RJ45
CRT
RTC Conn.
MiniCard



USB 0	USB Conn.
USB 1	USB Conn.
USB 2	Bluetooth
USB 3	
USB 4	CMOS Camera
USB 5	Card Reader
USB 6	WiMax
USB 7	
USB 8	
USB 9	
USB 10	USB Conn.
USB 11	

IO BOARD - 01

HDMI Conn.
USB Conn.x2
MIC-IN Conn.
Head Phone Conn.
Audio IC
Card Reader IC
Card Reader Conn.



ASUS

ASUSTek COMPUTER INC.

Title : B TO B CONNECTOR

Engineer: Jack Hsu

Size Custom

Project Name UL50AT


Date: Friday, October 16, 2009

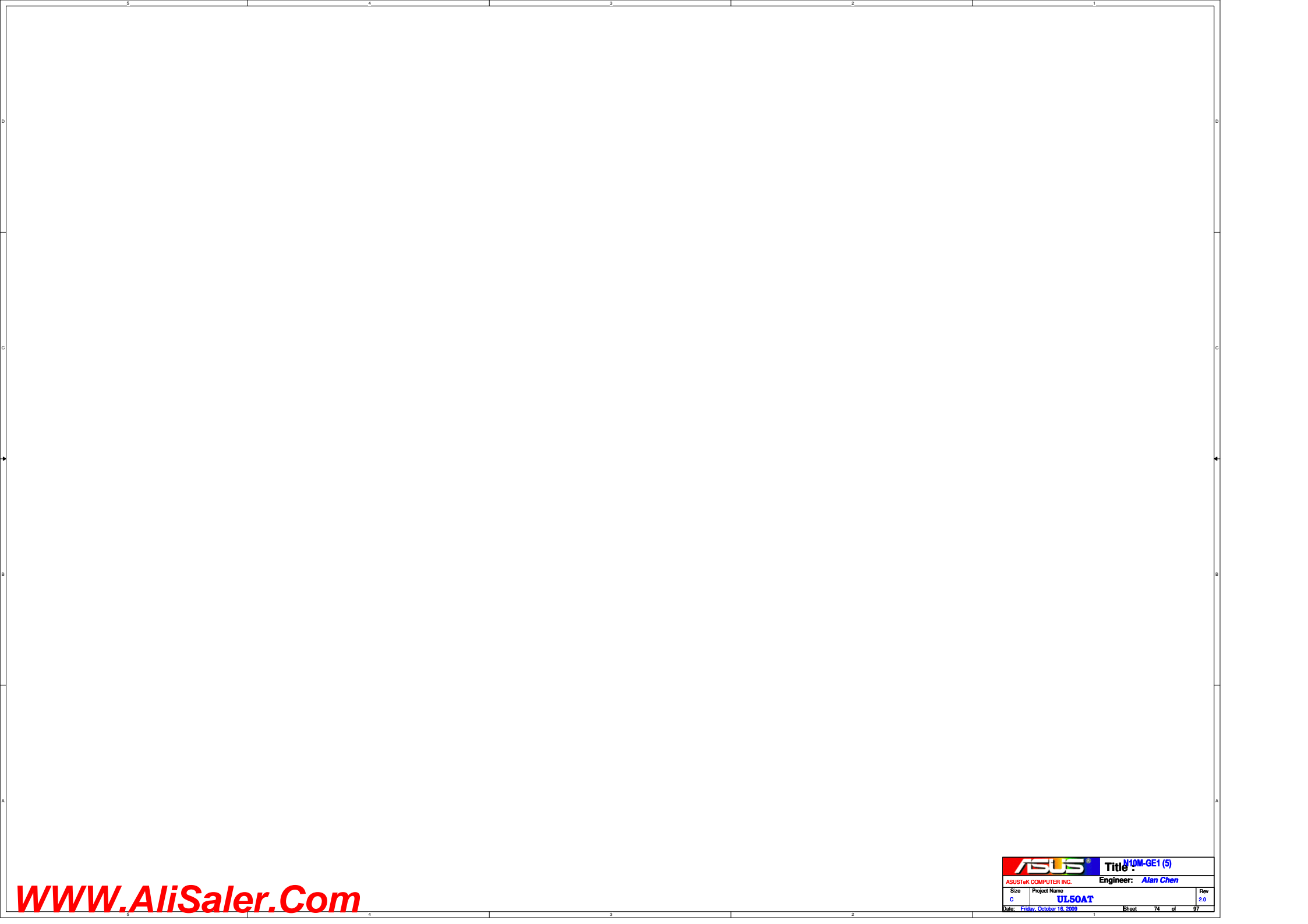
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Rev 2.0





		Title : M10M-GE1 (4)	
ASUSTeK COMPUTER INC.		Engineer: Alan Chen	
Size	Project Name		Rev
C	UL50AT		2.0
Date: Friday, October 16, 2009		Sheet	78 of 97

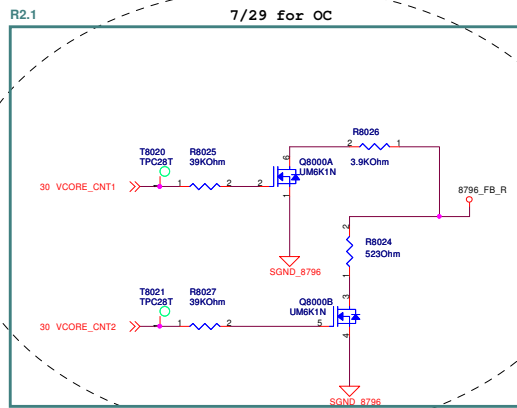




5	4	3	2	1
D				D
C				C
B				B
A				A
5	4	3	2	1

		Title: <Title>	
ASUSTeK COMPUTER INC.		Engineer: Alan Chen	
Size	Project Name	Rev	
C	UL50AT <Variant Name>	2.0	
Date: Friday, October 16, 2009		Sheet	77 of 97

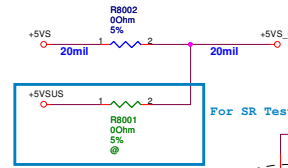
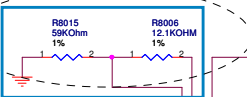




CPU
VID=1.2V

Vcore_CNT1	Vcore_CNT2	Voltage	Offset
H	H	1.3988V	VID+222mV
H	L	1.3488V	VID+26mV
L	H	1.25V	VID+196mV
L	L	1.2V	VID

modify 10/15 for OC



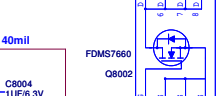
Modify 05/18



modify 10/15 for OC



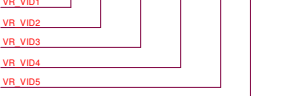
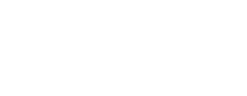
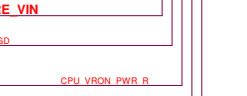
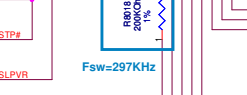
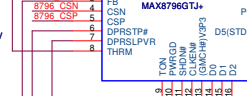
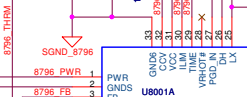
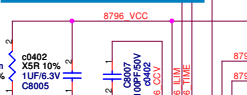
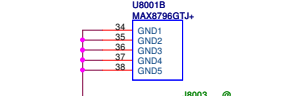
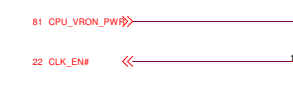
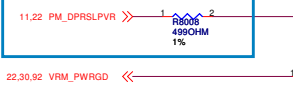
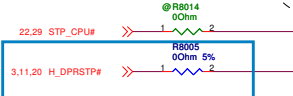
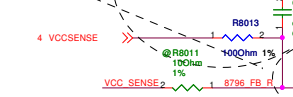
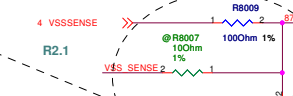
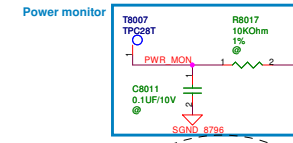
Modify 08/06



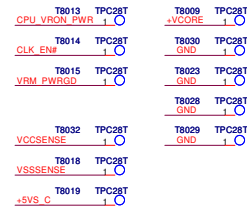
modify 10/15 for OC



modify 10/15 for OC



Total count: 37 pcs



<Variant Name>

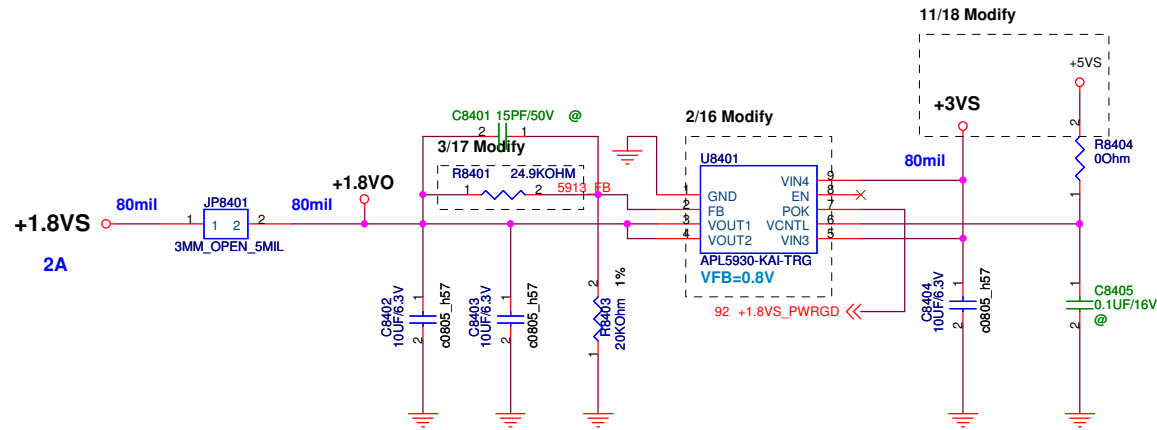
ASUS Title : POWER_VCORE

ASUSTeK COMPUTER INC. CH/Engineer:

Size Project Name UL50AT Rev 2.0

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+1.8VS



T8401	TPC28T
+1.8VO	1
T8402	TPC28T
+1.8VS	1
T8403	TPC28T
GND	1
T8404	TPC28T
GND	1

<Variant Name>

ASUS		Title : POWER_IO_+1.8VS	
ASUSTeK COMPUTER INC.		Engineer: CH/Fred	
Size	Project Name	Rev	
Custom	UL50AT	2.0	
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	5	4	3	2	1
D					
C					
B					
A					

<Variant Name>

		Title : <Title>	
ASUSTeK COMPUTER INC.		Engineer: CH/Fred	
Size Custom	Project Name UL50AT		Rev 2.0
Date: Friday, October 16, 2009		Sheet	86 of 97

D

C

B

A

<Variant Name>



Title : <Title>

ASUSTeK COMPUTER INC.

Engineer: *CH/Fred*

Size
A

Project Name

UL50AT

Rev
2.0

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D

C

B

A

<Variant Name>



Title : <Title>

ASUSTeK COMPUTER INC.

Engineer: *CH/Fred*

Size

A

Project Name

UL50AT

Rev

2.0

Date: Friday, October 16, 2009

Sheet

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of

97

5

4

3

2

1

D

D

C

C

B

B

A

A

4

3

2

1

<Variant Name>



Title :POWER_DETECT

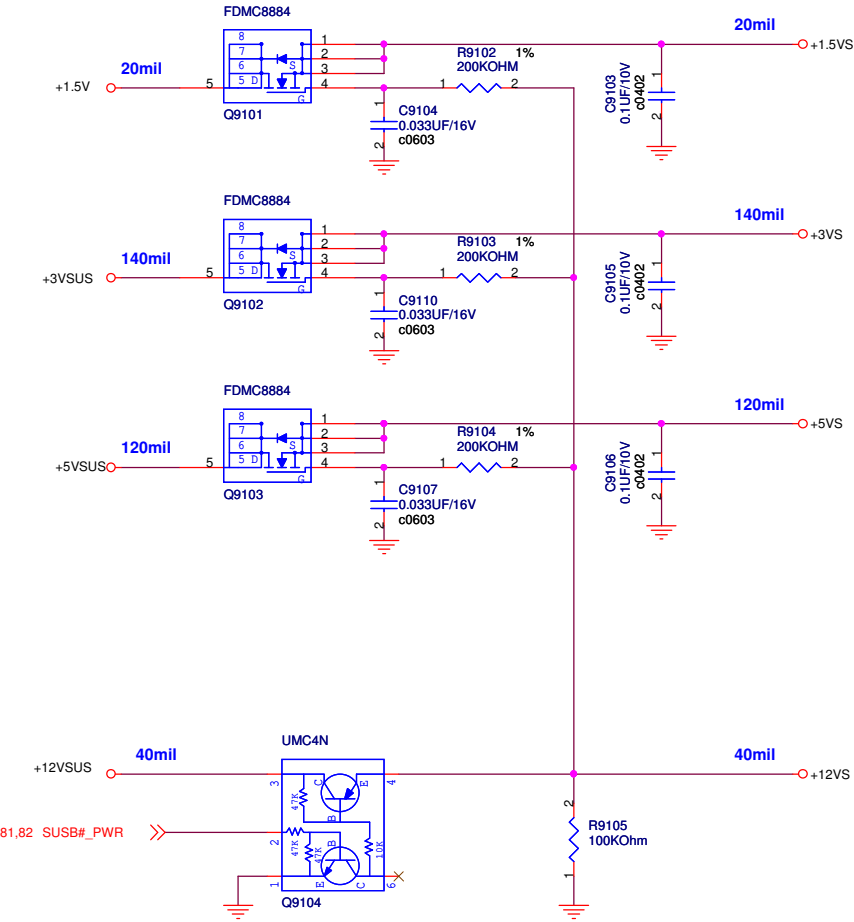
ASUSTeK COMPUTER INC.

Engineer: CH/Fred

Size	Project Name	Rev
Custom	UL50AT	2.0

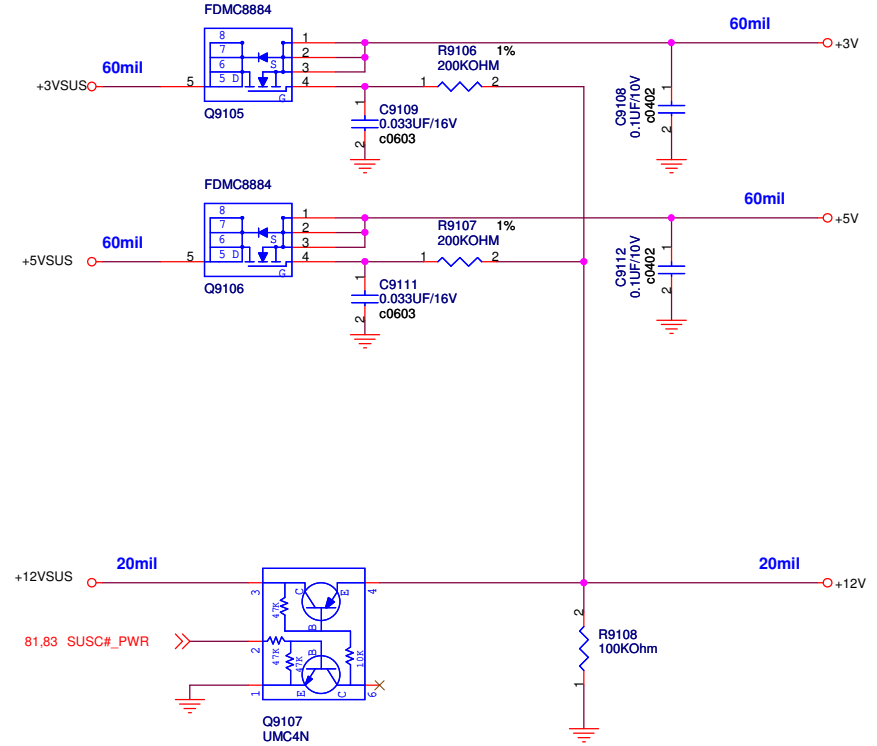
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SUSB#_PWR POWER




Total count: 19 pcs

SUSC#_PWR POWER

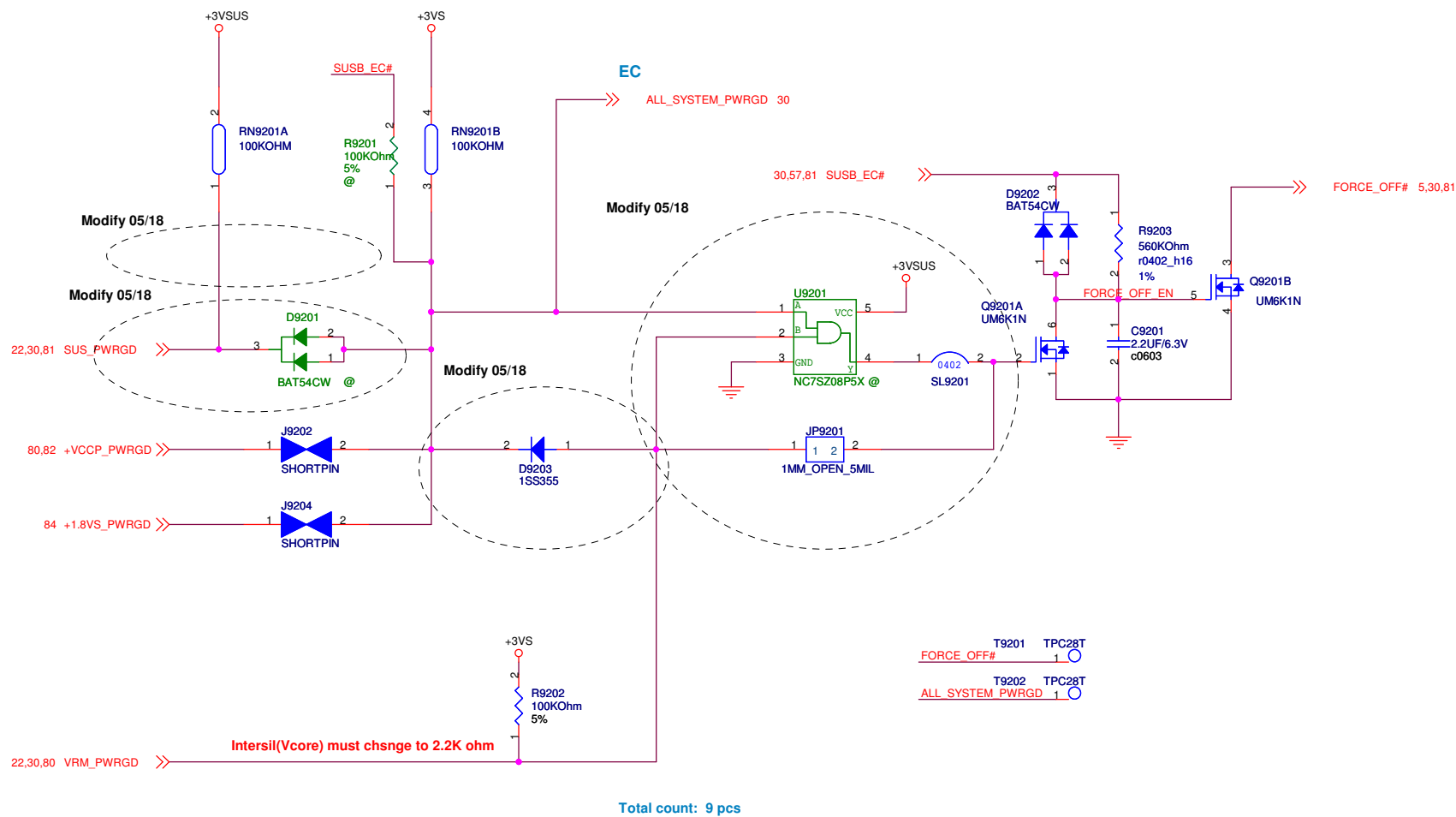


T9101	TPC28T	T9111	TPC28T
+12VSUS	1	+3VSUS	1
T9102	TPC28T	T9113	TPC28T
+12VS	1	+3VS	1
T9103	TPC28T	T9115	TPC28T
+12V	1	+3V	1
T9104	TPC28T	T9120	TPC28T
+5VSUS	1	+1.5V	1
T9106	TPC28T	T9121	TPC28T
+5VS	1	+1.5VS	1
T9110	TPC28T	T9123	TPC28T
+5V	1	SUSC#_PWR1	1
		T9114	TPC28T
		SUSC#_PWR1	1

<Variant Name>

		Title : POWER_LOAD SWITCH	
ASUSTeK COMPUTER INC.		Engineer: CH/Fred	
Size B	Project Name UL50AT		Rev 2.0
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POWER GOOD DETECTOR



<Variant Name>



Title :POWER_PROTECT

ASUSTeK COMPUTER INC.

Engineer: *CH/Fred*

Size	Project Name
B	

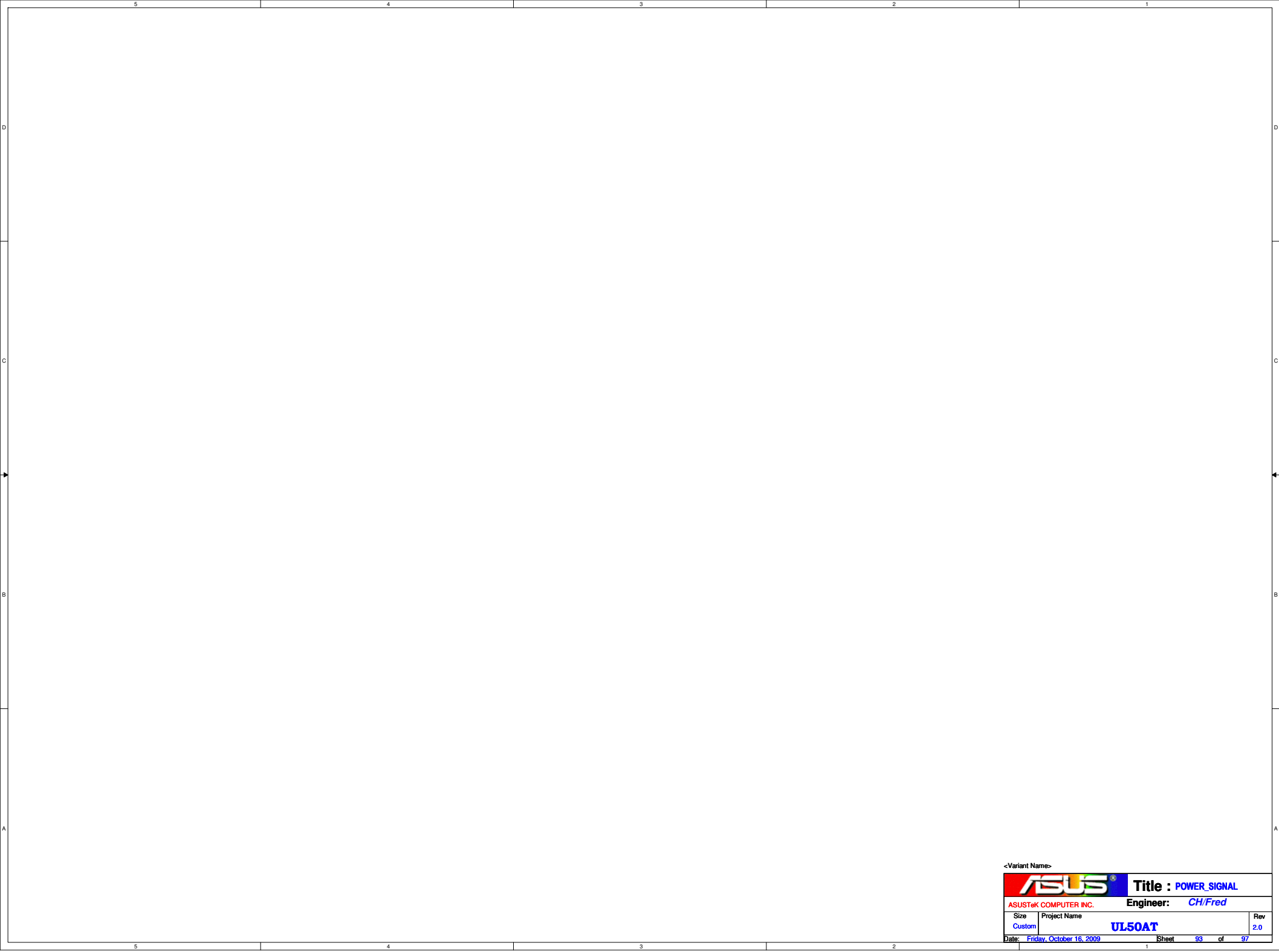
Project Name	
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UL50AT


Rev	2.0
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<Variant Name>



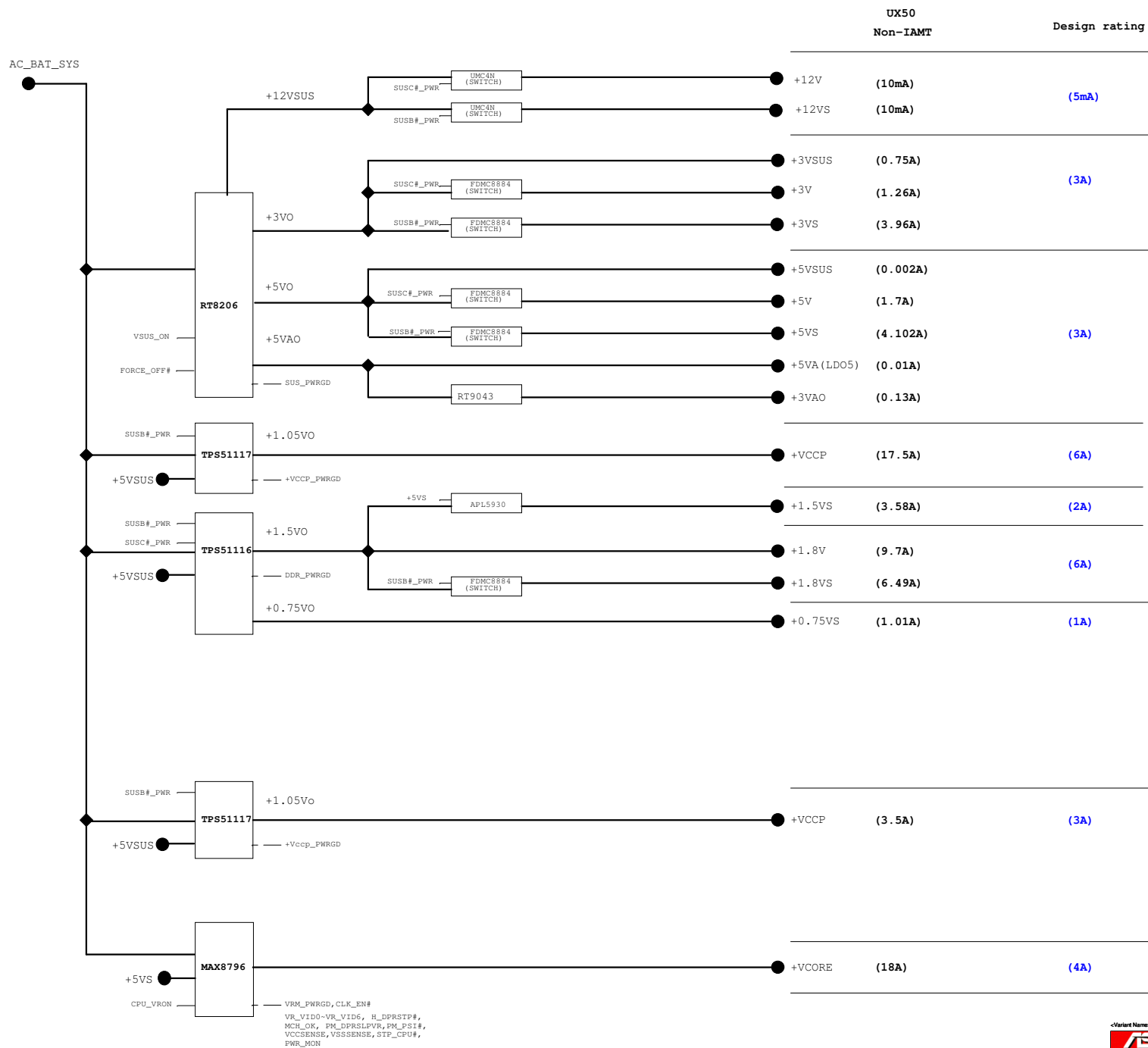
Title : POWER_SIGNAL

ASUSTeK COMPUTER INC.

Engineer: CH/Fred

Size	Project Name	Rev
Custom	UL50AT	2.0

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	5	4	3	2	1
D					
C					
B					
A	<div> <div><Variant Name></div> <div> <div> <div>ASUS®</div> <div>Title : <Title></div> </div> <div> <div>ASUSTeK COMPUTER INC.</div> <div>Engineer: CH/Fred</div> </div> <div> <div> <div>Size</div> <div>A</div> </div> <div> <div>Project Name</div> <div>UL50AT</div> </div> <div> <div>Rev</div> <div>2.0</div> </div> </div> <div> <div>Date: Friday, October 16, 2009</div> <div> <div>Sheet</div> <div>95</div> <div>of</div> <div>97</div> </div> </div> </div> </div>				
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Rev	Date	Description
1.00		First Release!
1.10		
2.00		

